CLAIMS

1. A method for displaying frames, said method comprising:

providing a first frame;

waiting to receive information about a second frame to display, after displaying the first frame; and

providing the first frame, if the information regarding the second frame is not received before a predetermined time.

2. The method of claim 1, further comprising:

providing the second frame if the information regarding the second frame is received by the predetermined time.

3. The method of claim 1, wherein the predetermined time comprises a first horizontal synchronization pulse following a vertical synchronization pulse associated with the second frame.

4. The method of claim 1, wherein the information comprises an address of a memory location, wherein the memory location at the address stores a starting pixel for the second frame.

5. The method of claim 1, further comprising:

receiving information regarding the first frame; and

storing the information regarding the first frame.

6. The method of claim 5, wherein providing the first frame if the information regarding the second frame is not received before the predetermined time further comprises providing the first frame based on the information regarding the first frame, and wherein the method further comprises:

overwriting the information regarding the first frame with the information regarding the second frame and providing the second frame based on the information regarding the second frame, if the information regarding the second frame is received before the predetermined time.

7. The method of claim 1, wherein providing the first frame further comprises:

rasterizing the first frame.

8. A system for displaying frames, said system comprising:

a display engine for providing a first frame;

a host processor for providing information about a second frame to the display engine, after the display engine provides the first frame; and

wherein the display engine provides the first frame, if host processor does not provide the information regarding the second frame to the display engine before a predetermined time.

9. The system of claim 8, wherein the display engine provides the second frame if the host processor provides the information regarding the second frame before the predetermined time.

10. The system of claim 8, wherein the predetermined time comprises a first horizontal synchronization pulse following a vertical synchronization pulse associated with the second frame.

11. The system of claim 8, further comprising:

a frame buffer for storing the second frame beginning at least one starting address; and

wherein the information comprises the at least one starting address.

12. The system of claim 8, further comprising:

a first at least one register for storing the information regarding the first frame.

13. The system of claim 12, further comprising:

a feeder for providing the first frame based on the information regarding the first frame if the host processor does not provide the information regarding the second frame before the predetermined time.

14. The system of claim 13, wherein the host processor overwrites the information regarding the first frame with the information regarding the second frame and wherein the feeder providing the second frame based on the information regarding the second frame.

15. The system of claim 13, wherein the feeder rasterizes the first frame.

16. A feeder for providing a frame, said feeder comprising:

a first one or more registers for storing one or more starting address for a first frame;

a circuit for calculating starting addresses for one or more rows of the first frame following a vertical synchronization pulse associated with the first frame;

a host processor for writing one or more starting address for a second frame to the first one or more registers; and

wherein the first one or more registers stores the one or more starting address for the first frame until the host processor writes the one or more starting address for the second frame to the first one or more registers.

17. The feeder of claim 16, further comprising:

a second one or more registers for storing the starting addresses for one or more rows of the first frame, following the vertical synchronization pulse associated with the first frame; and

wherein the circuit for calculating the starting address for one or more rows increments the starting address stored in the second one or more registers.

18. The feeder of claim 17, wherein the second one or more registers stores the starting addresses for one or more rows of the second frame following a vertical synchronization pulse associated with the second frame, and wherein the circuit calculates the starting address for one or more rows of the second frame following the vertical synchronization pulse associated with the second frame, if the host processor writes the one or more starting address

to the first one or more registers before a predetermined time.

19. The feeder of claim 17, wherein the second one or more registers stores the starting address for one or more rows of the first frame following a vertical synchronization pulse associated with the second frame, and wherein the circuit calculates the starting address for one or more rows of the first frame following the vertical synchronization pulse associated with the second frame, if the host processor does not write the one or more starting address to the first one or more registers before the predetermined time.

20. The feeder of claim 19, wherein the predetermined time is at a first horizontal synchronization pulse following the vertical synchronization pulse associated with the second frame.